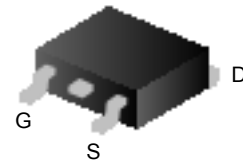
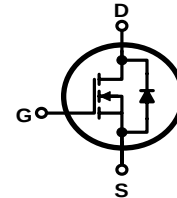


Features:

- ☐ Low Intrinsic Capacitances.
- ☐ Excellent Switching Characteristics.
- ☐ Extended Safe Operating Area.
- ☐ Unrivalled Gate Charge :Qg=6.8nC (Typ.).
- ☐ BVDSS=600V,I_D=2A
- ☐ R_{DS(on)} : 4.5 Ω (Max) @V_G=10V
- ☐ 100% Avalanche Tested



Schematic diagram



Marking Diagram

- Y = Year
A = Assembly Location
WW = Work Week
VA = Version & Assembly plant
FIR2N60AL = Specific Device Code

Absolute Maximum Ratings (Ta=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-Source Voltage	600	V
I _D	Drain Current	T _j =25°C	2
		T _j =100°C	1.25
V _{GS(TH)}	Gate Threshold Voltage	±30	V
E _{AS}	Single Pulse Avalanche Energy (note1)	120	mJ
I _{AR}	Avalanche Current (note2)	2	A
P _D	Power Dissipation (T _j =25°C)	44	W
T _j	Junction Temperature(Max)	150	°C
T _{stg}	Storage Temperature	-55~+150	°C
TL	Maximum lead temperature for soldering purpose,1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJC}	Thermal Resistance,Junction to Case	-	2.84	°C/W
R _{θJA}	Thermal Resistance,Junction to Ambient	-	110	°C/W

Electrical Characteristics (Ta=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0	600	-	-	V
△BVDSS/△T _J	Breakdown Voltage Temperature Coefficient	I _D =250μA ,Reference to 25℃	-	0.6	-	V/℃
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V	-	-	1	μA
		V _{DS} =480V, T _j =125℃			10	
I _{GSSF}	Gate-body leakage Current, Forward	V _{GS} =+30V, V _{DS} =0V	-	-	100	nA
I _{GSSR}	Gate-body leakage Current, Reverse	V _{GS} =-30V, V _{DS} =0V	-	-	-100	
On Characteristics						
V _{GS(TH)}	Date Threshold Voltage	I _D =250μA,V _{DS} =V _{GS}	2	-	4	V
R _{DS(ON)}	Static Drain-Source On-Resistance	I _D =1A,V _{GS} =10V	-	-	4.5	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0, f=1.0MHz	-	298	-	pF
C _{oss}	Output Capacitance		-	40	-	
C _{rss}	Reverse Transfer Capacitance		-	5	-	
Switching Characteristics						
T _{d(on)}	Turn-On Delay Time	V _{DD} =300V, I _D =2A R _G =25Ω (Note 3,4)	-	10	-	ns
Tr	Turn-On Rise Time		-	24	-	
T _{d(off)}	Turn-Off Delay Time		-	20	-	
T _f	Turn-Off Rise Time		-	25	-	
Q _g	Total Gate Charge	V _{DS} =480V,V _{GS} =10V, I _D =2A (Note 3,4)	-	6.8	-	nC
Q _{gs}	Gate-Source Charge		-	2.0	-	
Q _{gd}	Gate-Drain Charge		-	1.8	-	
Drain-Source Diode Characteristics and Maximum Ratings						
I _s	Max. Diode Forward Current	-	-	-	2	A
I _{SM}	Max. Pulsed Forward Current	-	-	-	8	
V _{SD}	Diode Forward Voltage	I _D =2A	-	-	1.5	V
T _{rr}	Reverse Recovery Time	I _S =2A,V _{GS} =0V diF/dt=100A/μs	-	380	-	nS
Q _{rr}	Reverse Recovery Charge	(Note3)	-	0.9	-	μC

Notes : 1, L=55mH, IAS=2A, VDD=50V, RG=25Ω, Starting TJ =25°C
 2, Repetitive Rating : Pulse width limited by maximum junction temperature
 3, Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
 4, Essentially Independent of Operating Temperature

Typical Characteristics

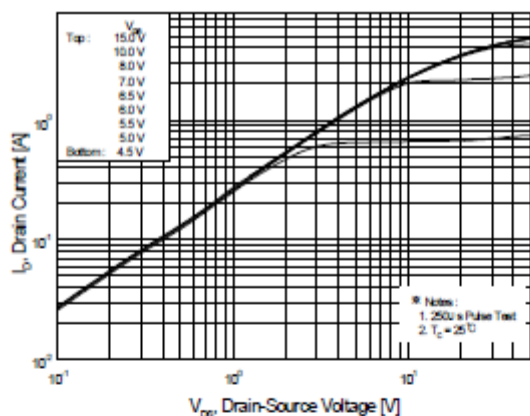


Figure 1. On-Region Characteristics

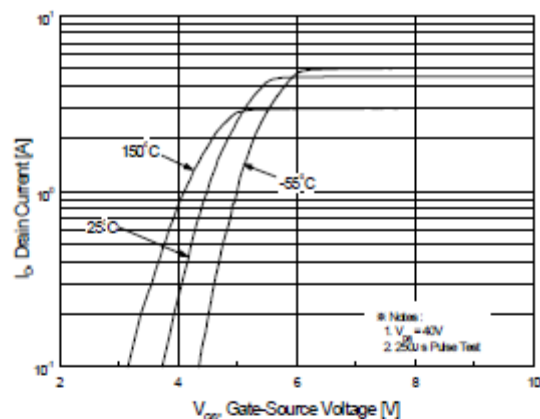


Figure 2. Transfer Characteristics

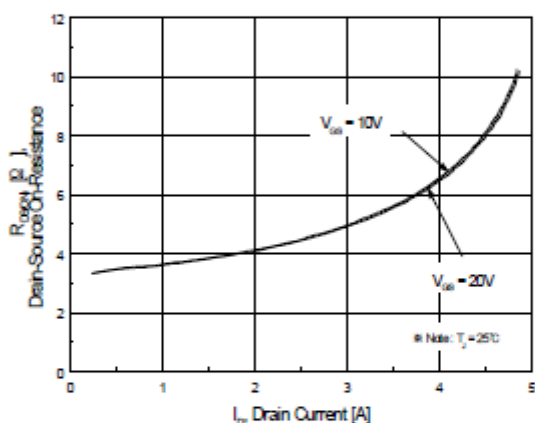


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

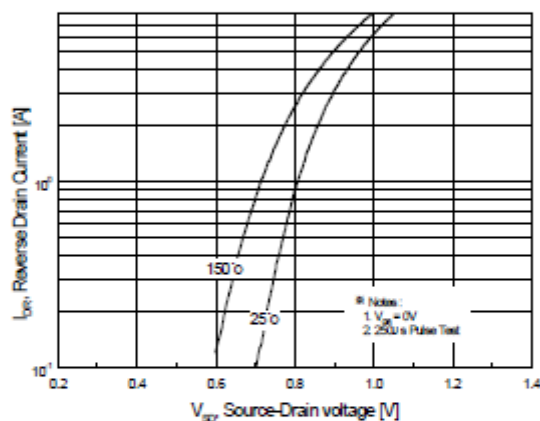


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

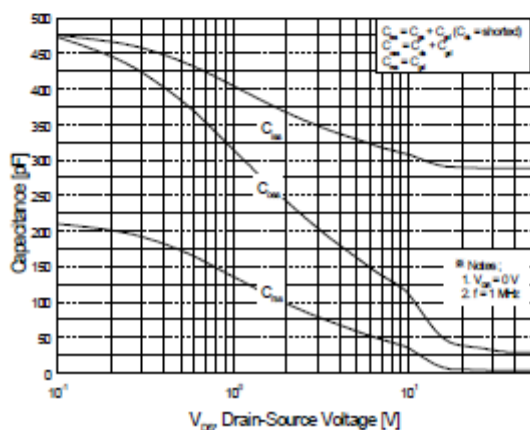


Figure 5. Capacitance Characteristics

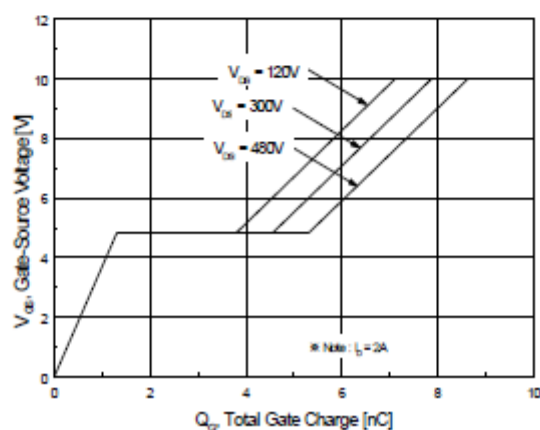


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

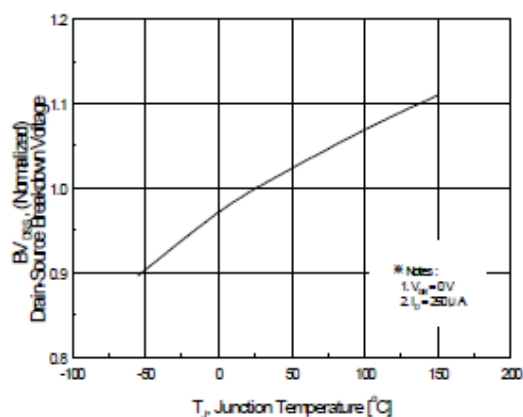


Figure 7. Breakdown Voltage Variation vs Temperature

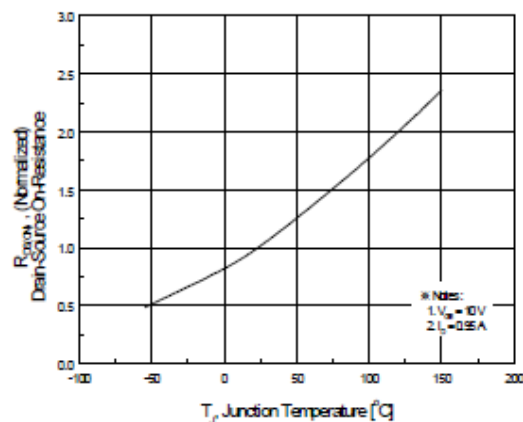


Figure 8. On-Resistance Variation vs Temperature

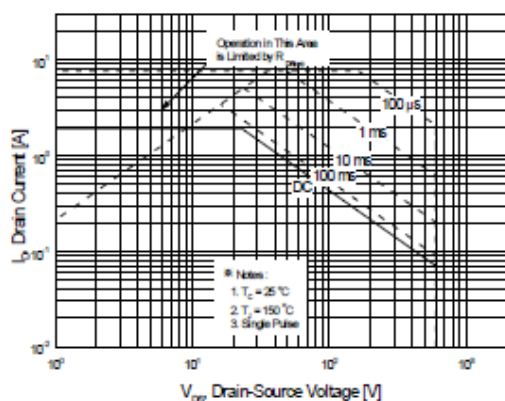


Figure 9. Maximum Safe Operating Area

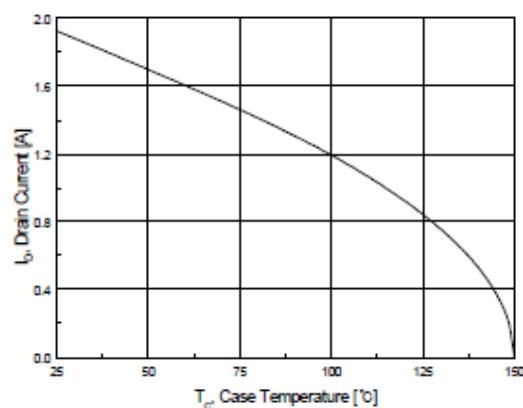


Figure 10. Maximum Drain Current vs Case Temperature

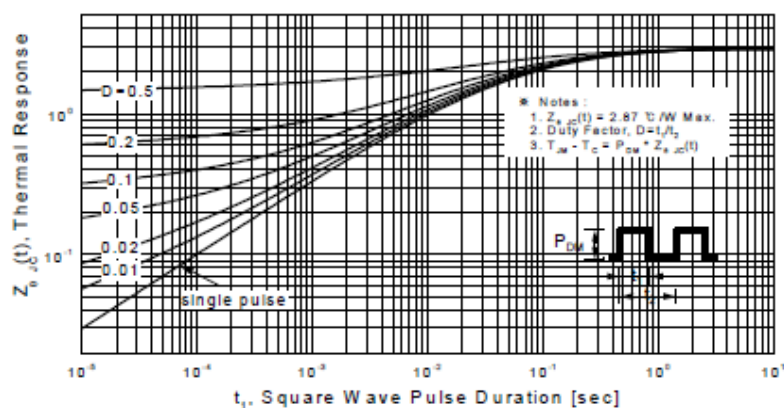
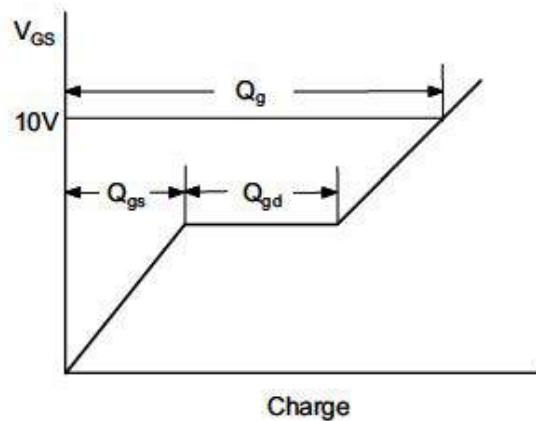
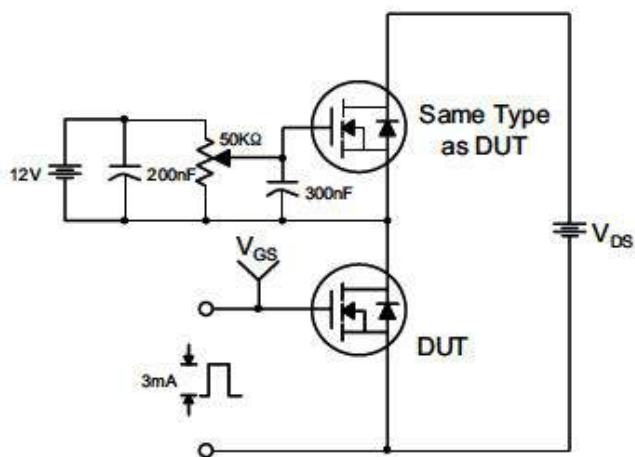
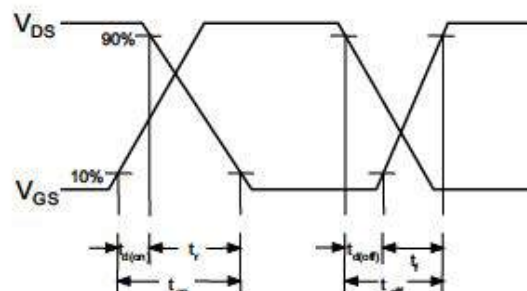
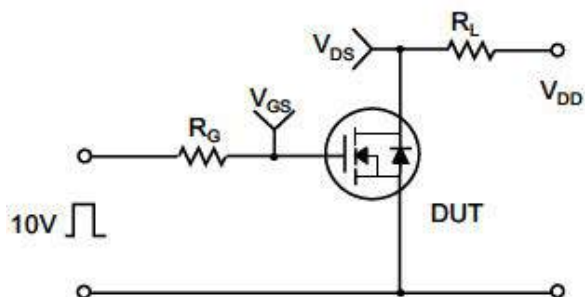
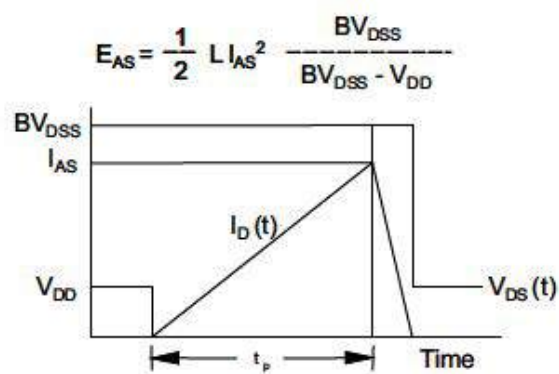
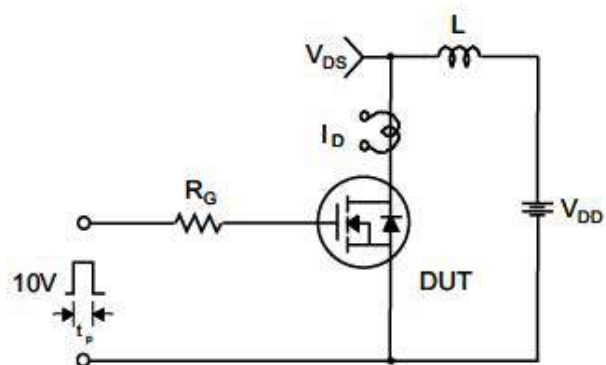


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms


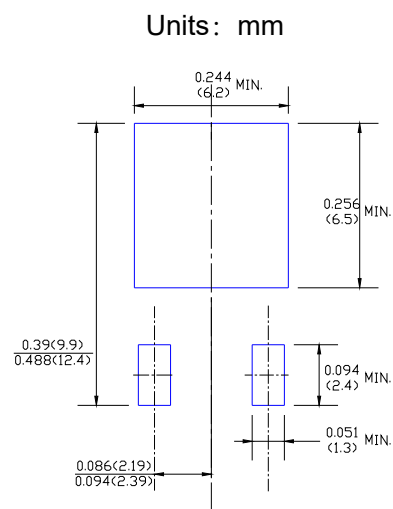
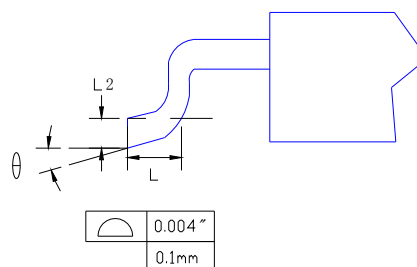
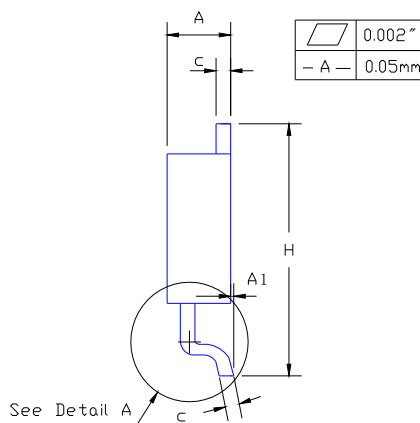
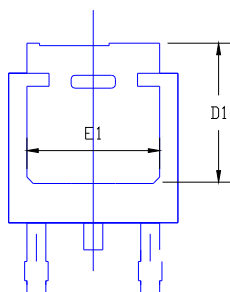
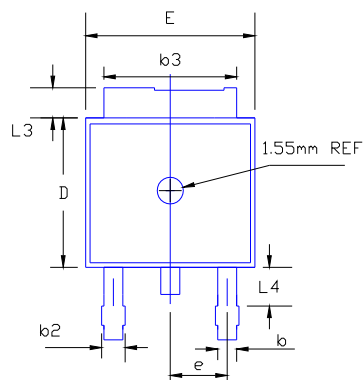
The diagram illustrates a switching transient test setup for a MOSFET Device Under Test (DUT). The DUT is represented by a MOSFET symbol with its gate connected to a driver circuit, its drain connected to a load inductor L , and its source connected to ground. The drain voltage is labeled V_{DS} and the source-drain current is labeled I_{SD} . The driver circuit consists of a MOSFET labeled "Driver" (noted as "Same Type as DUT") with its gate driven by a square-wave pulse V_{GS} through a gate resistor R_G . The driver's drain is connected to the DUT's gate. A supply voltage V_{DD} is connected to the drain of the driver and one end of the inductor L . The other end of the inductor L is connected to the DUT's drain. Two bullet points specify the control parameters:

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



TO-252

Package Dimension



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	
A1	-	0.005	-	0.13	
b	0.025	0.035	0.64	0.89	
b2	0.033	0.045	0.84	1.14	
b3	0.205	0.215	5.21	5.46	
c	0.018	0.024	0.46	0.61	
D	0.241	0.249	6.12	6.32	
D1	0.205	-	5.21	-	
E	0.250	0.265	6.35	6.73	
E1	0.190	-	4.83	-	
e	0.090 BSC.		2.29 BSC.		
H	0.380	0.410	9.65	10.41	
L	0.055	0.070	1.40	1.78	
L2	0.020 BSC.		0.51 BSC.		
L3	0.035	0.050	0.89	1.27	
L4	0.025	0.040	0.64	1.01	
θ	0°	8°	0°	8°	



Declaration

- Yixinwei reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
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- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	