N-Channel Power MOSFET

600V, 1A, 10Ω

FEATURES

- Advanced planar process
- 100% avalanche tested
- Low $R_{DS(ON)}$ 8Ω (Typ.)
- Low gate charge typical @ 6.1 nC (Typ.)
- Low Crss typical @4.2pF (Typ.)

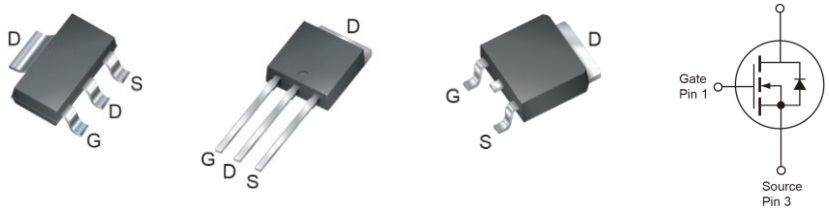
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	600	V
$R_{DS(on)}$ (max)	10	Ω
Q_g	6.1	nC

APPLICATION

- Power Supply
- Lighting
- Charger

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOT-223 **TO-251 (IPAK)** **TO-252 (DPAK)**



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK), SOT-223 per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER		SYMBOL	IPAK/DPAK	SOT-223	UNIT
Drain-Source Voltage		V_{DS}	600		V
Gate-Source Voltage		V_{GS}	±30		V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	1		A
	T_C = 100°C		0.7		
Pulsed Drain Current (Note 2)		I_{DM}	4		A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	39	2.1	W
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	5		mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	1		A
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5		V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.87	--	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	110	60	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 5)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	600	--	--	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 0.5A	$R_{DS(ON)}$	--	8	10	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2.5	3.5	4.5	V
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	10	μA
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Forward Transfer Conductance	V_{DS} = 10V, I_D = 0.5A	g_{fs}	--	0.8	--	S
Dynamic (Note 6)						
Total Gate Charge	V_{DS} = 480V, I_D = 1A, V_{GS} = 10V	Q_g	--	6.1	--	nC
Gate-Source Charge		Q_{gs}	--	1.4	--	
Gate-Drain Charge		Q_{gd}	--	3.3	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	138	--	pF
Output Capacitance		C_{oss}	--	17.1	--	
Reverse Transfer Capacitance		C_{rss}	--	4.2	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	12.5	--	Ω
Switching (Note 7)						
Turn-On Delay Time	V_{DD} = 300V, R_G =25Ω I_D = 1A, V_{GS} = 10V	$t_{d(on)}$	--	7.7	--	ns
Turn-On Rise Time		t_r	--	6.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	15.3	--	
Turn-Off Fall Time		t_f	--	14.9	--	
Source-Drain Diode (Note 5)						
Diode Forward Voltage	I_S = 1A, V_{GS} = 0V	V_{SD}	--	0.9	1.4	V
Source Current	Integral reverse diode In the MOSFET	I_S	--	--	1	A
Source Current (Pulse)		I_{SM}	--	--	4	

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. L = 10mH, I_{AS} = 1A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C.
4. I_{SD}≤1A , V_{DD}≤BV_{DSS} , di/dt≤200A/us , Starting T_J = 25°C.
5. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%.
6. For DESIGN AID ONLY, not subject to production testing.
7. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

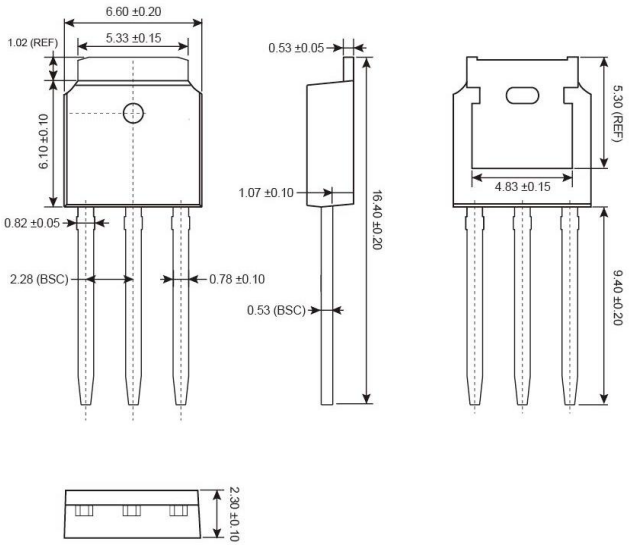
PART NO.	PACKAGE	PACKING
TSM1NB60CH C5G	TO-251	75 pcs / Tube
TSM1NB60CP ROG	TO-252	2,500 pcs / 13” Reel
TSM1NB60CW RPG	SOT-223	2,500 pcs / 13” Reel

Note:

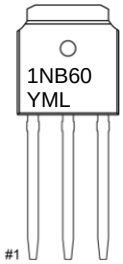
1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251



MARKING DIAGRAM



Y = Year Code
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L = Lot Code (1~9, A~Z)

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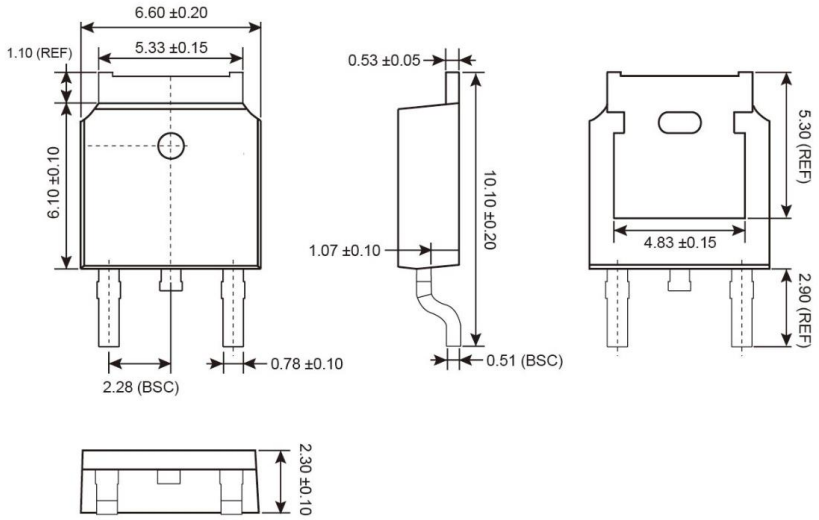
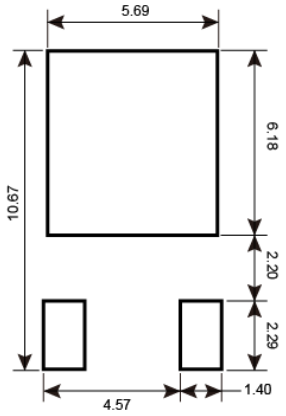


SUGGESTED PAD LAYOUT



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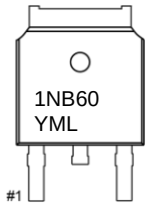

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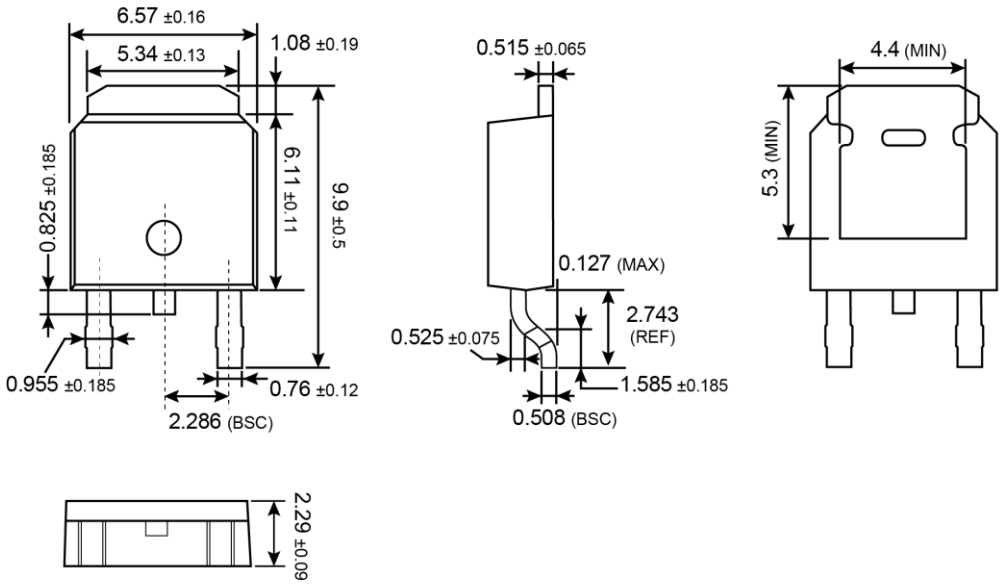

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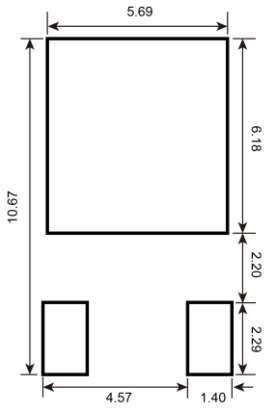

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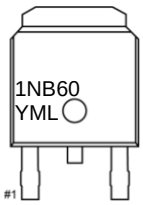

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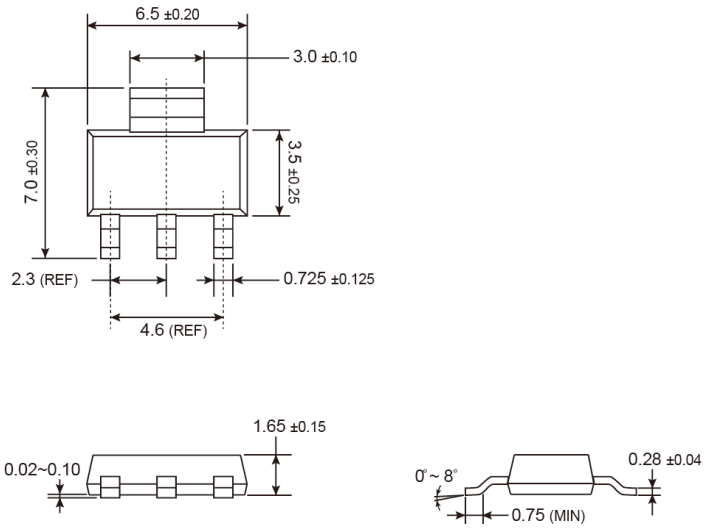

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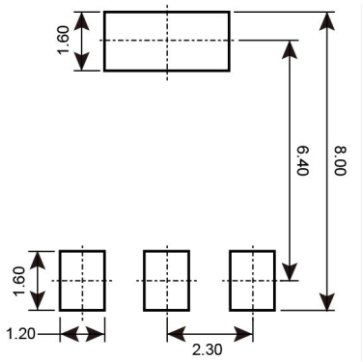

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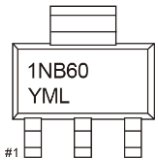

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