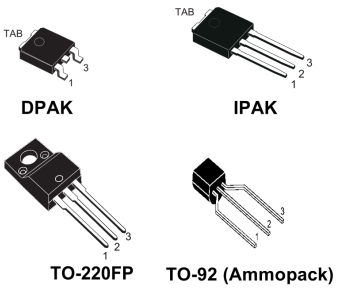
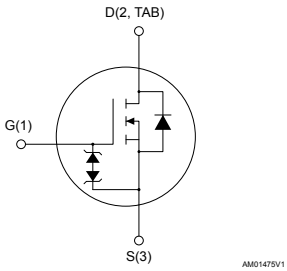
STD2HNK60Z, STD2HNK60Z-1
STF2HNK60Z, STQ2HNK60ZR-AP

Datasheet

N-channel 600 V, 3.5 Ω typ., 2 A Power MOSFETs in DPAK, IPAK, TO-220FP and TO-92 packages





Features

Order code	V_{DS}	$R_{DS(on)}$max.	I_D	Package
STD2HNK60Z	600 V	4.8 Ω	2 A	DPAK
STD2HNK60Z-1				IPAK
STF2HNK60Z				TO-220FP
STQ2HNK60ZR-AP			0.5 A	TO-92

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Product status
STD2HNK60Z
STD2HNK60Z-1
STF2HNK60Z
STQ2HNK60ZR-AP

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK, IPAK	TO-220FP	TO-92	
V_{DS}	Drain-source voltage	600			V
V_{GS}	Gate-source voltage	±30			V
I_D	Drain current (continuous) at T_C = 25 °C	2.0	2.0 (1)	0.5	A
I_D	Drain current (continuous) at T_C = 100 °C	1.26	1.26 (1)	0.32	A
I_{DM} (2)	Drain current (pulsed)	8	8 (1)	2	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	20	3	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2			kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)		2500		V
dv/dt (3)	Peak diode recovery voltage slope	4.5			V/ns
T_j	Operating junction temperature range	-55 to 150			°C
T_{stg}	Storage temperature range				

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 2 A, di/dt ≤ 200 A/µs, V_{DSpeak} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK, IPAK	TO-220FP	TO-92	
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.77	6.25		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	100	62.5	120	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50			°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead			40	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	120	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1 A		3.5	4.8	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	280		pF
C_{oss}	Output capacitance			38		
C_{rss}	Reverse transfer capacitance			7		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	30		pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 2 A, V_{GS} = 0 to 10 V (see Figure 18. Test circuit for gate charge behavior)	-	11	15	nC
Q_{gs}	Gate-source charge			2.25		
Q_{gd}	Gate-drain charge			6		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)	-	10	-	ns
t_r	Voltage rise time			30		
$t_{d(off)}$	Turn-off delay time			23		
t_f	Fall time			50		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
I_{SDM} (1)	Source-drain current (pulsed)				8	
V_{SD} (2)	Forward on voltage	I_{SD} = 2 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs	-	178		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 20 V (see Figure 19. Test circuit for inductive load switching and diode recovery times)		445		nC
I_{RRM}	Reverse recovery current			5		A
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs	-	200		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 20 V, T_j = 150 °C (see Figure 19. Test circuit for inductive load switching and diode recovery times)		500		nC
I_{RRM}	Reverse recovery current			5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area forDPAK/IPAK

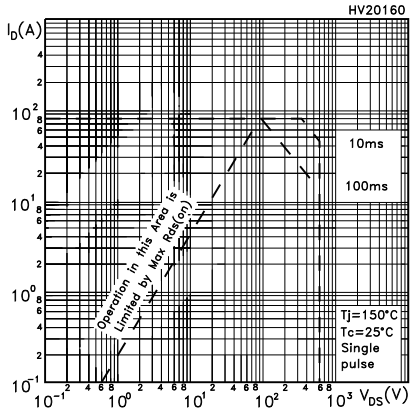


Figure 2. Thermal impedance for DPAK/IPAK

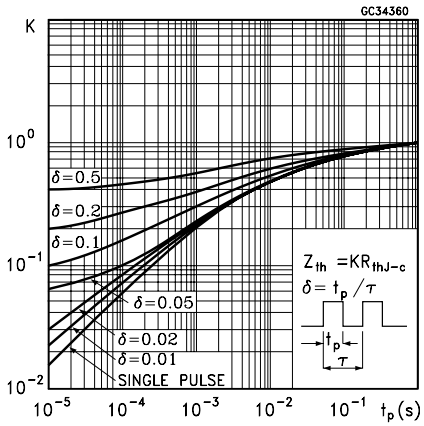


Figure 3. Safe operating area for TO-220FP

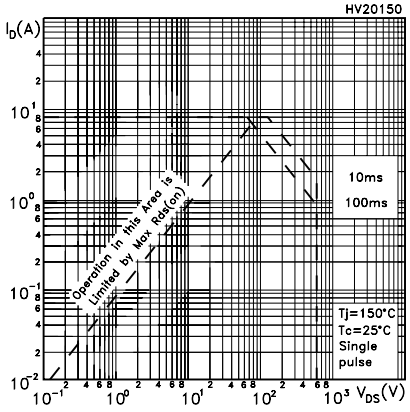


Figure 4. Thermal impedance for TO-220FP

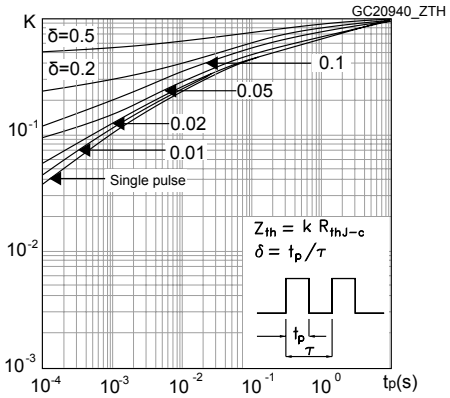


Figure 5. Safe operating area for TO-92

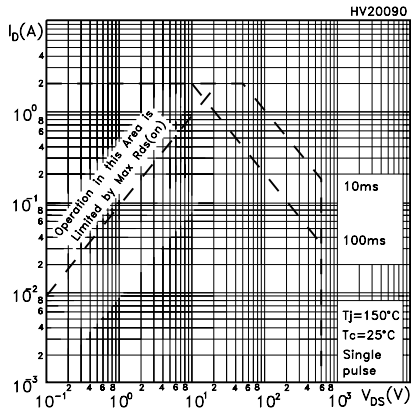


Figure 6. Thermal impedance for TO-92

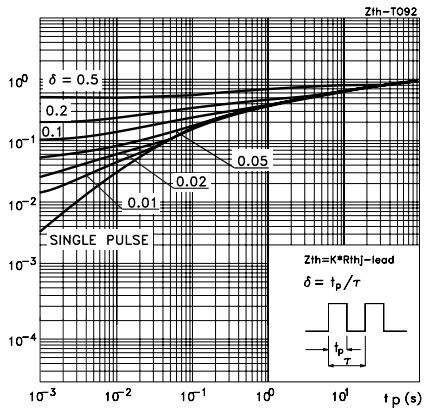


Figure 7. Output characterisics

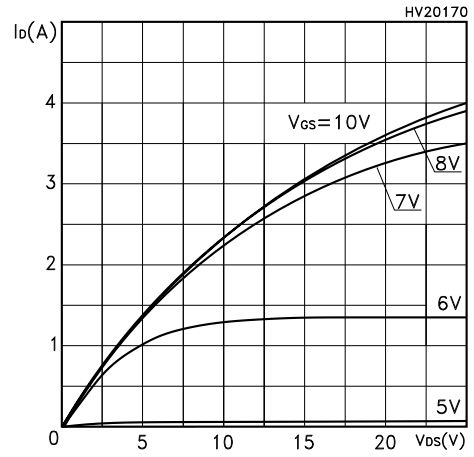


Figure 8. Transfer characteristics

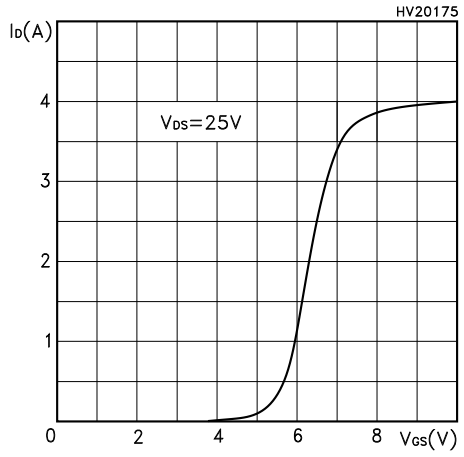


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

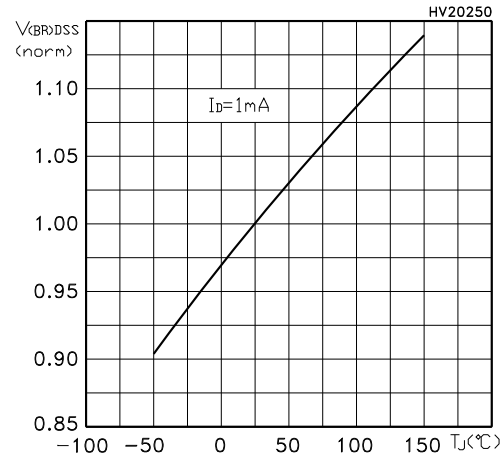


Figure 10. Static drain-source on-resistance

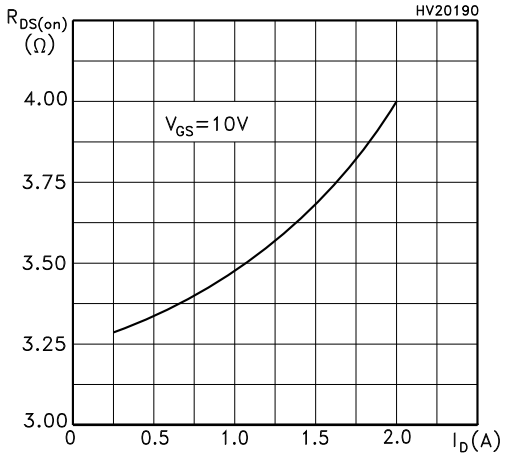


Figure 11. Gate charge vs gate-source voltage

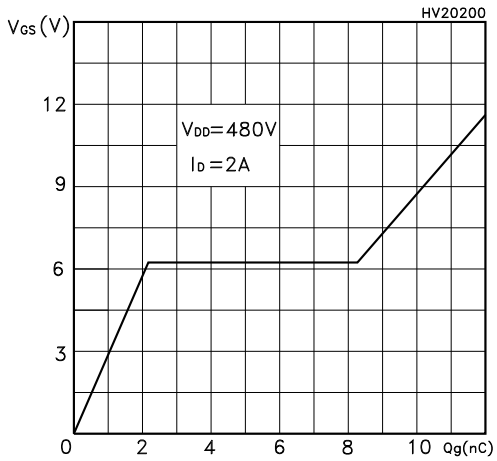


Figure 12. Capacitance variations

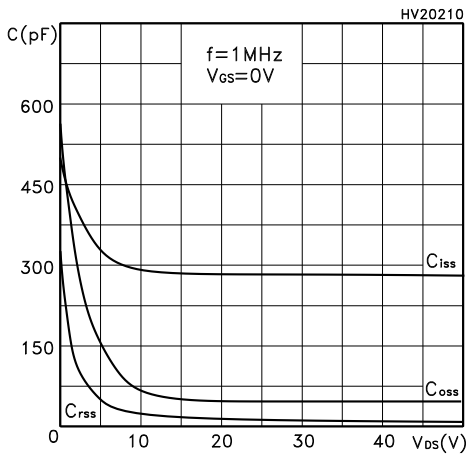


Figure 13. Normalized gate threshold voltage vs temperature

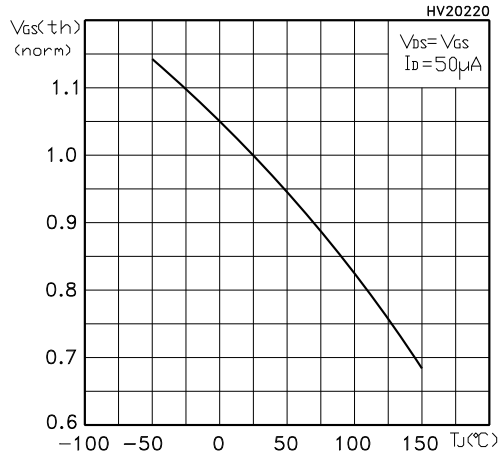


Figure 14. Normalized on-resistance vs temperature

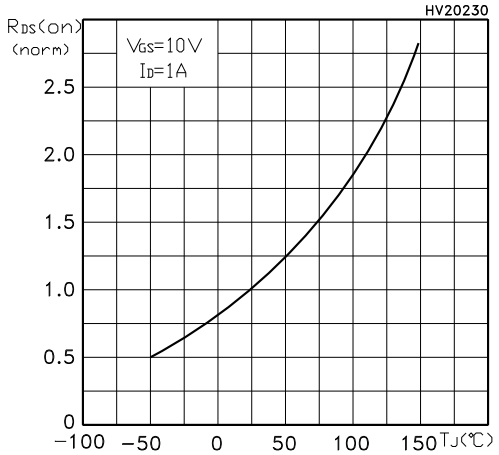


Figure 15. Source-drain diode forward characteristics

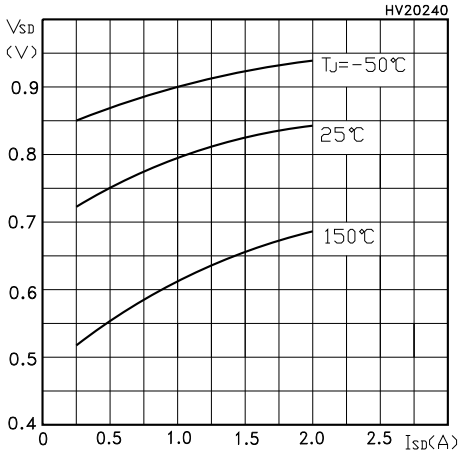
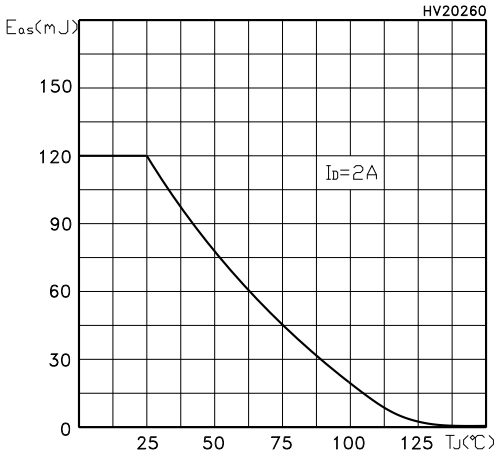


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Test circuit for resistive load switching times

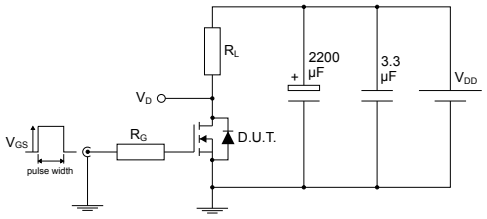


Figure 18. Test circuit for gate charge behavior

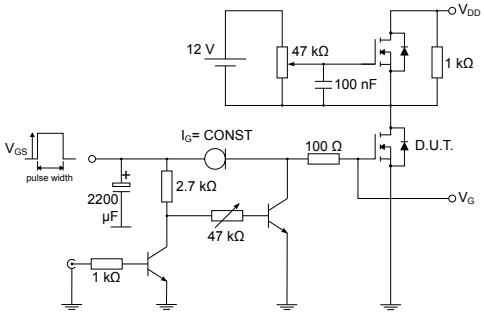


Figure 19. Test circuit for inductive load switching and diode recovery times

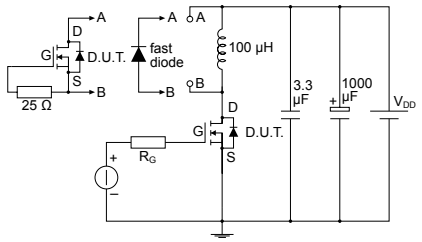


Figure 20. Unclamped inductive load test circuit

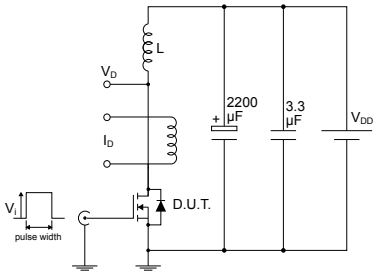


Figure 21. Unclamped inductive waveform

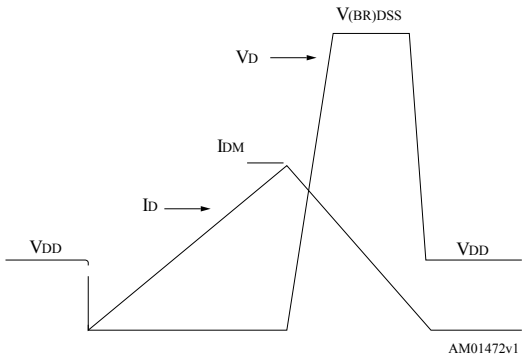


Figure 22. Switching time waveform