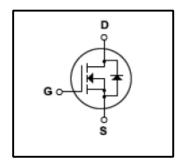
## SHENZHEN YIXINWEI TECHNOLOGY CO.,LTD

### Silicon N-Channel MOSFET

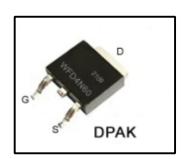
#### **Features**

- 4A,600V. $R_{DS(on)}(Max\ 2.5\Omega)@V_{GS}=10V$
- Ultra-low Gate Charge(Typical 16nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Isolation Voltage ( VISO = 4000V AC )
- Maximum Junction Temperature Range(150°C)



#### **General Description**

This Power MOSFET is produced using 's advanced Planar stripe, DMOS technology. This latest technology has Been Especially designed to minimize on-state resistance, have a high Rugged avalanche characteristics. This devices is specially well Suited for half bridge and full bridge resonant topology line a Electronic lamp ballast.



#### **Absolute Maximum Ratings**

Symbol	Parameter	Value	Units	
VDSS	Drain Source Voltage	600	V	
1-	Continuous Drain Current(@Tc=25℃)	4	А	
l <sub>D</sub>	Continuous Drain Current(@Tc=100℃)	2.5	А	
Ідм	Drain Current Pulsed (Note1	16	А	
Vgs	Gate to Source Voltage	±30	V	
Eas	Single Pulsed Avalanche Energy (Note 2)	240	mJ	
Ear	Repetitive Avalanche Energy (Note 1	) 10	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3	4.5	V/ns	
Pp	Total Power Dissipation(@Tc=25℃)	80	W	
PD	Derating Factor above 25 ℃	0.78	W/°C	
TJ, Tstg	Junction and Storage Temperature	-55~150	$^{\circ}$	
TL	Channel Temperature	300	C	

#### Thermal Characteristics

Cumbal	Dorameter	Value			Linita	
Symbol	Parameter	Min	Тур	Max	Units	
Rajc	Thermal Resistance, Junction-to-Case	-	-	1.56	°C/W	
RQJA	Thermal Resistance, Junction-to-Ambient*			50		
R <sub>QJA</sub>	Thermal Resistance, Junction-to-Ambient	-	-	110	°C/W	

<sup>\*</sup>When mounted on the minimum pad size recommended(PCB Mount)



# Electrical Characteristics (Tc = 25° C)

Charac	teristics	Symbol	Test Condition	Min	Туре	Max	Unit
Gate leakage cu	Gate leakage current		V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA
Gate-source bre	akdown voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = ±10 μA, V <sub>DS</sub> = 0 V	±30			V
Drain cut-off current		V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	10	μA
		IDSS	V <sub>DS</sub> = 480 V, T <sub>c</sub> = 125°C	-	-	100	μA
Drain-source breakdown voltage		V(BR)DSS	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	600	-	-	V
Gate threshold voltage		V <sub>GS(th)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> =250 μA	2	-	4	V
Drain-source Of	N resistance	RDS(ON)	Vgs = 10 V, ID =3.25A	-	1.8	2.5	Ω
Input capacitance		Ciss	V <sub>DS</sub> = 25 V,	-	545	670	
Reverse transfer capacitance		Crss	Vgs = 0 V,	-	7	10	pF
Output capacitance		Coss	f = 1 MHz	-	70	90	
	Rise time	tr	V <sub>DD</sub> =300 V,	-	10	30	
Occidentalism of the c	Turn-on time	ton	I <sub>D</sub> = 4.4 A	-	35	80	
Switching time	Fall time	tf	R <sub>G</sub> =25 Ω	-	45	100	ns
	Turn-off time	toff	(Note4,5)	-	20	50	
Total gate charge (gate-source			V <sub>DD</sub> = 480 V,		40	00	
plus gate-drain)		Qg	Vgs = 10 V,	-	16	20	
Gate-source charge		Qgs	I <sub>D</sub> =4.4A	-	3.4	-	nC
Gate-drain ("miller") Charge		Qgd	(Note4,5)	-	7	-	

## Source-Drain Ratings and Characteristics (Ta = 25° C)

Characteristics	Symbol	Test Condition	Min	Туре	Max	Unit
Continuous drain reverse current	IDR	-	-	-	4	Α
Pulse drain reverse current	IDRP	-	-	-	17.6	Α
Forward voltage (diode)	VDSF	IDR =4.4 A, VGS = 0 V	-	-	1.4	V
Reverse recovery time	trr	IDR = 4.4 A, VGS = 0 V,	-	390	-	ns
Reverse recovery charge	Qrr	dlor / dt = 100 A / μs	-	2.2	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=18.5mH,I\_AS=4.4A,V\_DD=50V,R\_G=0\Omega,Starting T\_J=25  $^{\circ}\mathrm{C}$ 

3.I $_{SD}$ ≤4A,di/dt≤200A/us, V $_{DD}$ <BV $_{DSS}$ ,STARTING T $_{J}$ =25  $^{\circ}$ C

4.Pulse Test: Pulse Width≤300us,Duty Cycle≤2%

 $5. Essentially independent of operating \ temperature.\\$ 

This transistor is an electrostatic sensitive device

Please handle with caution



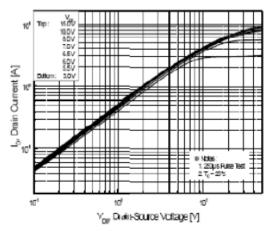


Fig.1 On-State Characteristics

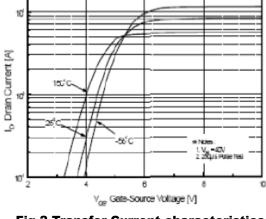


Fig.2 Transfer Current characteristics

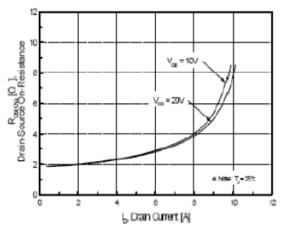


Fig3. On Resistance Variation vs
Drain current

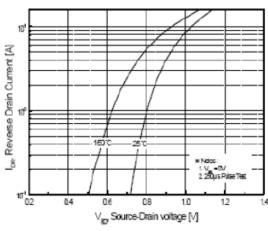


Fig.4 Body Diode Forward Voltage Variation vs Source Current and Temperature

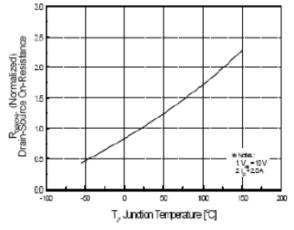


Fig.5 On-Resistance Variation vs

Junction Temperature

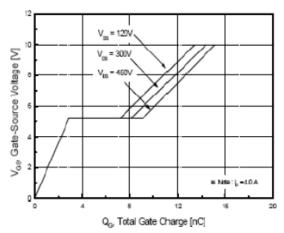


Fig.6 Gate Charge Characteristics



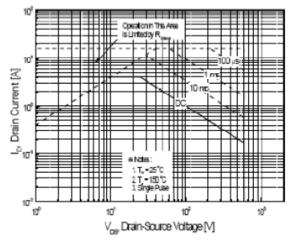


Fig.7 Maximum Safe Operation Area

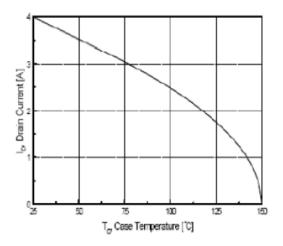


Fig.8 Maximum Drain Current vs Case Temperature

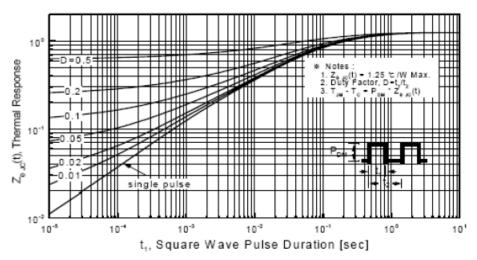


Fig.9 Transient Thermal Response curve



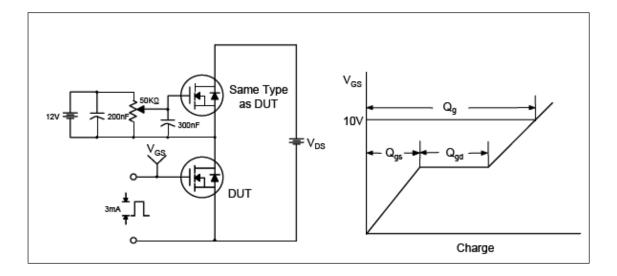


Fig.10 Gate Test Circuit & Waveform

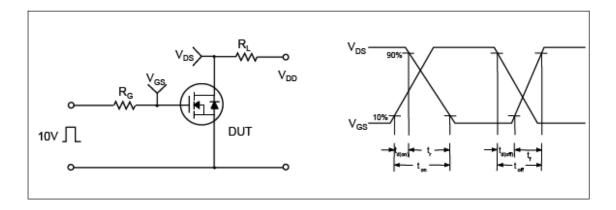


Fig.11 Resistive Switching Test Circuit & Waveform

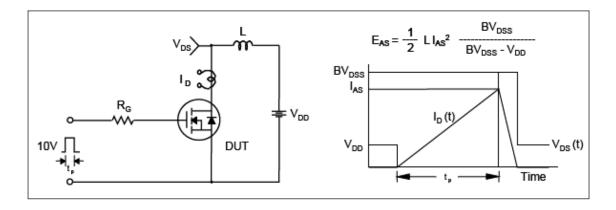


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform



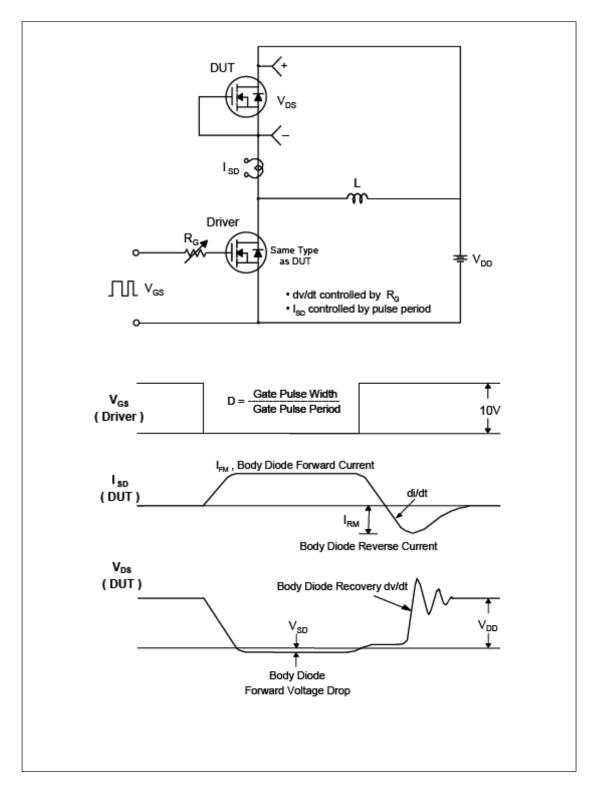


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-252 Package Dimension

