



Precision References

The TL431, A, B integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω . The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: $\pm 0.4\%$, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage

ORDERING INFORMATION

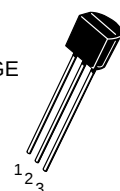
Device	Operating Temperature Range	Package
TL431CLP, ACLP, BCLP	$T_A = 0^\circ \text{ to } +70^\circ\text{C}$	TO-92
TL431CP, ACP, BCP		Plastic
TL431CDM, ACDM, BCDM		Micro-8
TL431CD, ACD, BCD		SOP-8
TL431ILP, AILP, BILP	$T_A = -40^\circ \text{ to } +85^\circ\text{C}$	TO-92
TL431IP, AIP, BIP		Plastic
TL431IDM, AIDM, BIDM		Micro-8
TL431ID, AID, BID		SOP-8

TL431, A, B Series

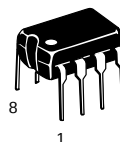
PROGRAMMABLE PRECISION REFERENCES

SEMICONDUCTOR TECHNICAL DATA

LP SUFFIX
PLASTIC PACKAGE
CASE 29
(TO-92)



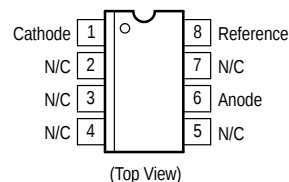
Pin 1. Reference
2. Anode
3. Cathode



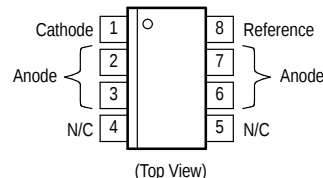
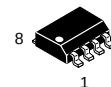
P SUFFIX
PLASTIC PACKAGE
CASE 626



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro-8)



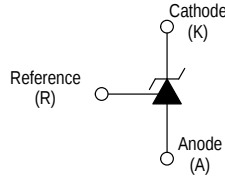
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)



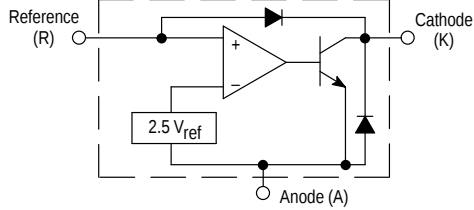
SOP-8 is an internally modified SO-8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 package.

TL431, A, B Series

Symbol

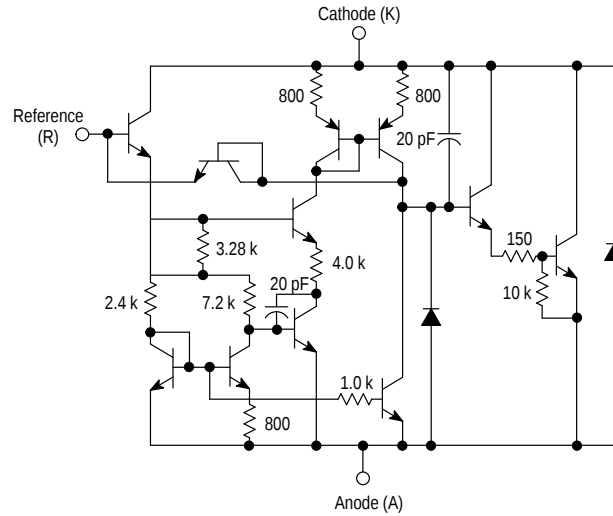


Representative Block Diagram



Representative Schematic Diagram

Component values are nominal



This device contains 12 active transistors.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	–100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	–0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC	T_A	–40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package DM Suffix Plastic Package	P_D	0.70 1.10 0.52	W
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package	P_D	1.5 3.0	W

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

THERMAL CHARACTERISTICS

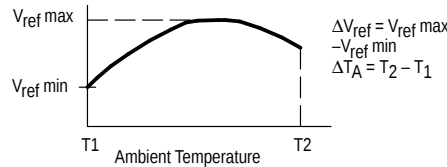
Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83	41	–	°C/W

TL431, A, B Series

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V _{KA} = V _{ref} , I _K = 10 mA T _A = 25°C T _A = T _{low} to T _{high} (Note 1)	V _{ref}	2.44 2.41	2.495 –	2.55 2.58	2.44 2.423	2.495 –	2.55 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) V _{KA} = V _{ref} , I _K = 10 mA	ΔV _{ref}	–	7.0	–	–	3.0	–	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I _K = 10 mA (Figure 2), ΔV _{KA} = 10 V to V _{ref} ΔV _{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	– –	–1.4 –1.0	–2.7 –2.0	– –	–1.4 –1.0	–2.7 –2.0	mV/V
Reference Input Current (Figure 2) I _K = 10 mA, R1 = 10 k, R2 = ∞ T _A = 25°C T _A = T _{low} to T _{high} (Note 1)	I _{ref}	– –	1.8 –	4.0 6.5	– –	1.8 –	4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I _K = 10 mA, R1 = 10 k, R2 = ∞	ΔI _{ref}	–	0.8	2.5	–	0.4	1.2	μA
Minimum Cathode Current For Regulation V _{KA} = V _{ref} (Figure 1)	I _{min}	–	0.5	1.0	–	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V _{KA} = 36 V, V _{ref} = 0 V	I _{off}	–	260	1000	–	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) V _{KA} = V _{ref} , ΔI _K = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z _{KA}	–	0.22	0.5	–	0.22	0.5	Ω

NOTES: 1. T_{low} = –40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM = 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM = +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
2. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C}$$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

3. The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

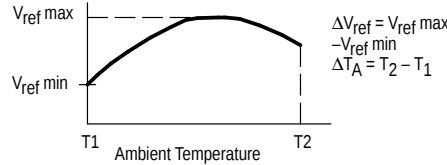
$$|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2} \right)$$

TL431, A, B Series

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI			TL431AC			TL431B			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V _{KA} = V _{ref} , I _K = 10 mA T _A = 25°C T _A = T _{low} to T _{high}	V _{ref}	2.47 2.44	2.495 –	2.52 2.55	2.47 2.453	2.495 –	2.52 2.537	2.483 2.475	2.495 2.495	2.507 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) V _{KA} = V _{ref} , I _K = 10 mA	ΔV _{ref}	–	7.0	–	–	3.0	–	–	3.0	–	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I _K = 10 mA (Figure 2), ΔV _{KA} = 10 V to V _{ref} ΔV _{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	– –	–1.4 –1.0	–2.7 –2.0	– –	–1.4 –1.0	–2.7 –2.0	– –	–1.4 –1.0	–2.7 –2.0	mV/V
Reference Input Current (Figure 2) I _K = 10 mA, R1 = 10 k, R2 = ∞ T _A = 25°C T _A = T _{low} to T _{high} (Note 1)	I _{ref}	– –	1.8 –	4.0 6.5	– –	1.8 –	4.0 5.2	– –	1.1 –	2.0 4.0	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I _K = 10 mA, R1 = 10 k, R2 = ∞	ΔI _{ref}	–	0.8	2.5	–	0.4	1.2	–	0.4	1.2	μA
Minimum Cathode Current For Regulation V _{KA} = V _{ref} (Figure 1)	I _{min}	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V _{KA} = 36 V, V _{ref} = 0 V	I _{off}	–	260	1000	–	260	1000	–	230	500	nA
Dynamic Impedance (Figure 1, Note 3) V _{KA} = V _{ref} , ΔI _K = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z _{KA}	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

- NOTES:** 1. T_{low} = –40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM = 0°C for TL431ACP, TL431ACL, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM = +70°C for TL431ACP, TL431ACL, TL431CP, TL431CLP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
2. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C}$$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

3. The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2} \right)$$

TL431, A, B Series

Figure 1. Test Circuit for $V_{KA} = V_{ref}$

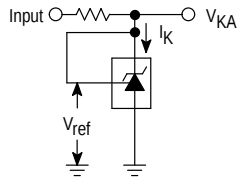


Figure 2. Test Circuit for $V_{KA} > V_{ref}$

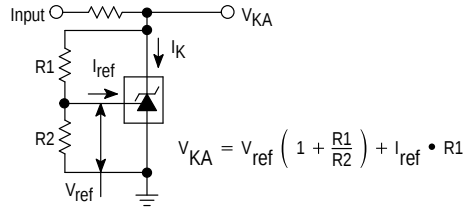


Figure 3. Test Circuit for I_{off}

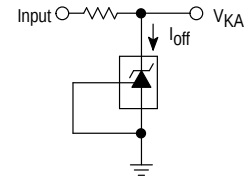


Figure 4. Cathode Current versus Cathode Voltage

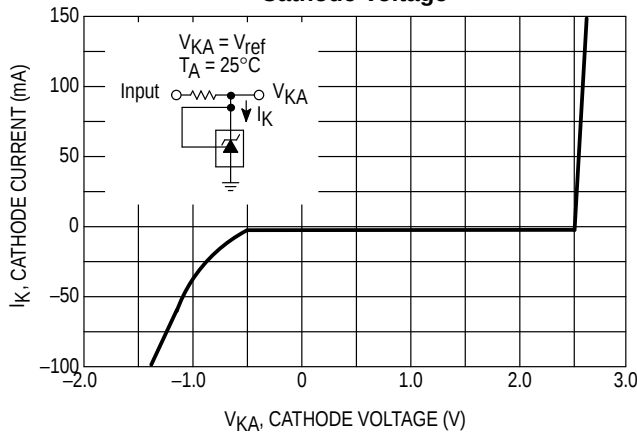


Figure 5. Cathode Current versus Cathode Voltage

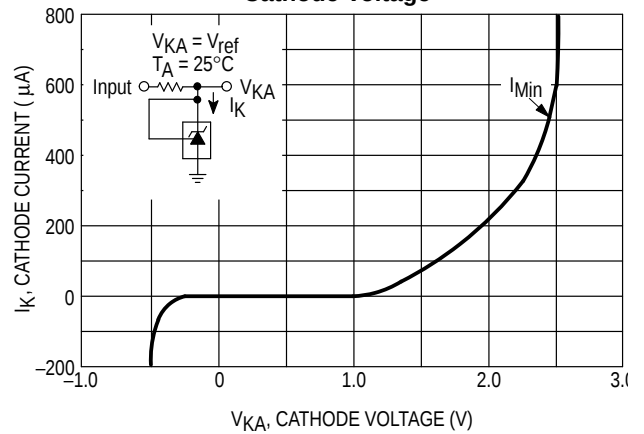


Figure 6. Reference Input Voltage versus Ambient Temperature

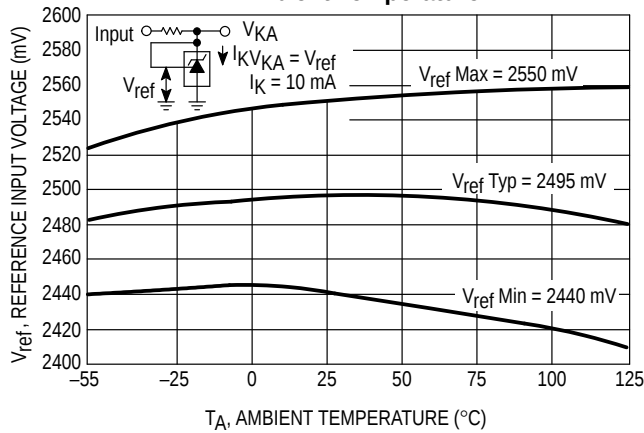
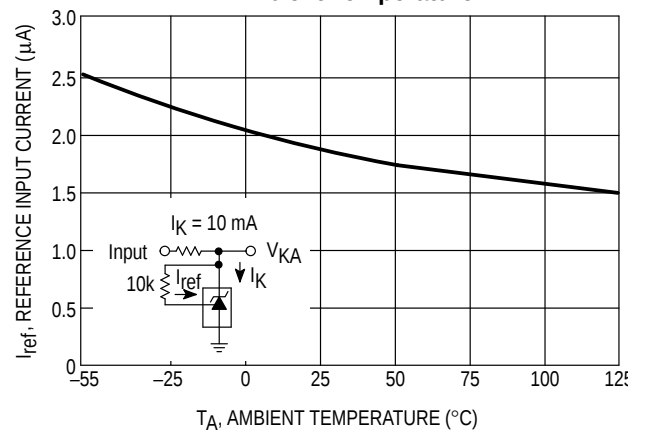


Figure 7. Reference Input Current versus Ambient Temperature



TL431, A, B Series

Figure 8. Change in Reference Input Voltage versus Cathode Voltage

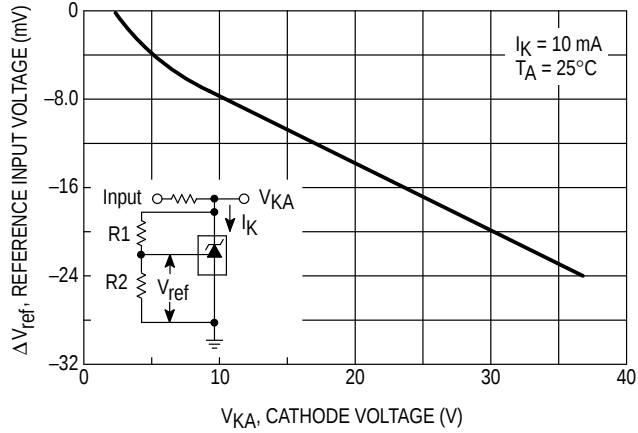


Figure 9. Off-State Cathode Current versus Ambient Temperature

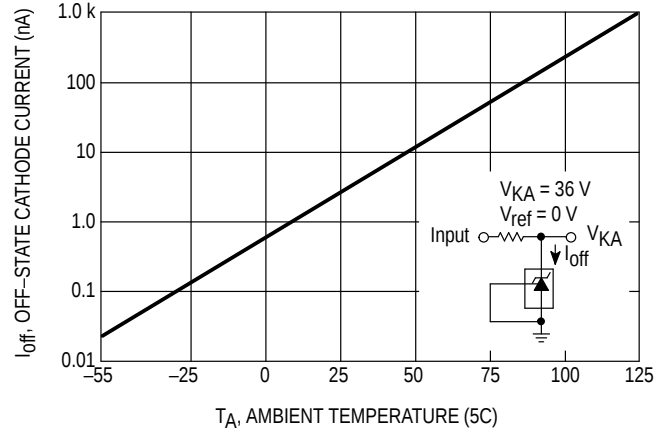


Figure 10. Dynamic Impedance versus Frequency

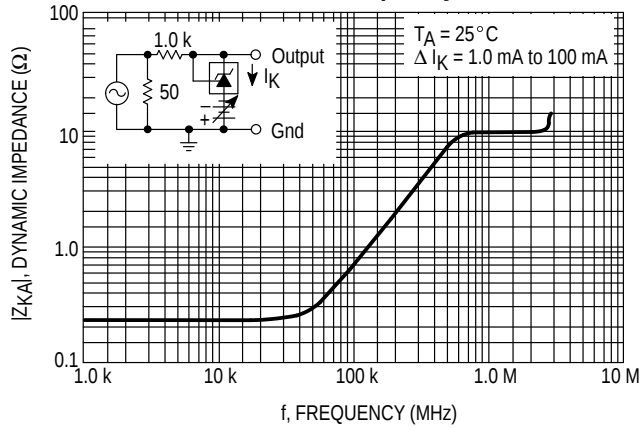


Figure 11. Dynamic Impedance versus Ambient Temperature

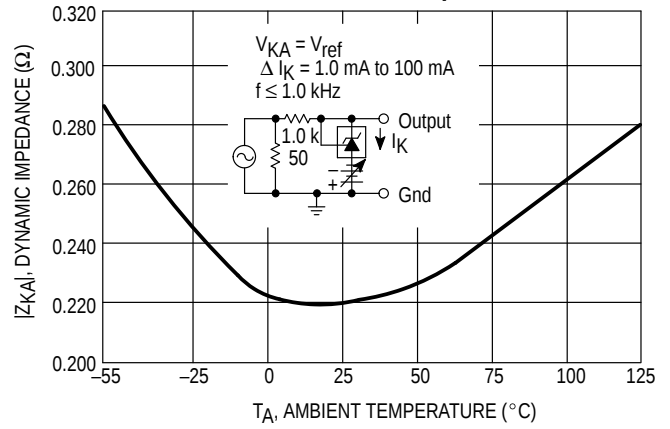


Figure 12. Open-Loop Voltage Gain versus Frequency

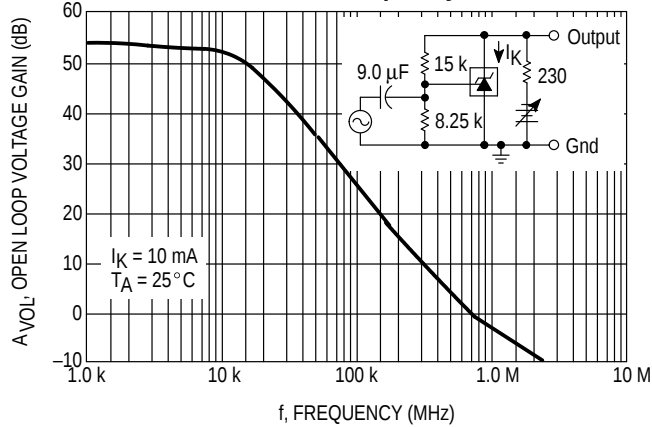
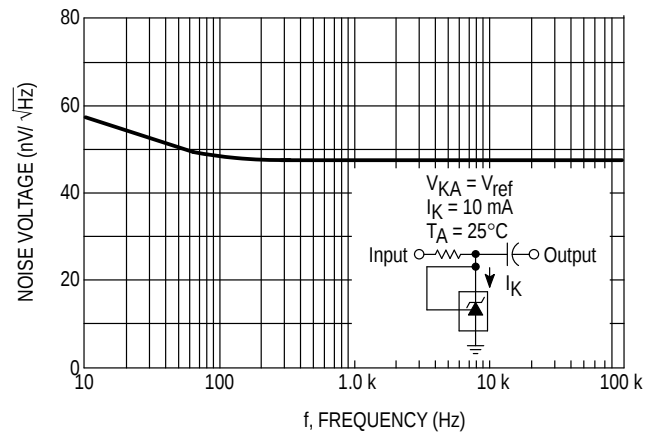


Figure 13. Spectral Noise Density



TL431, A, B Series

Figure 31. Simplified TL431 Device Model

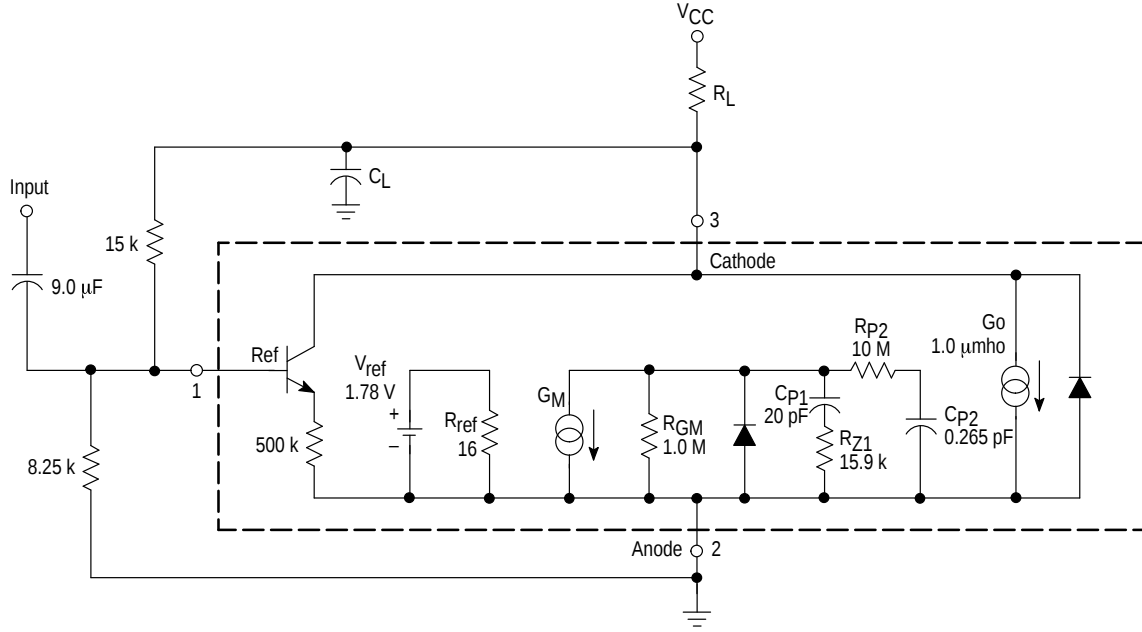
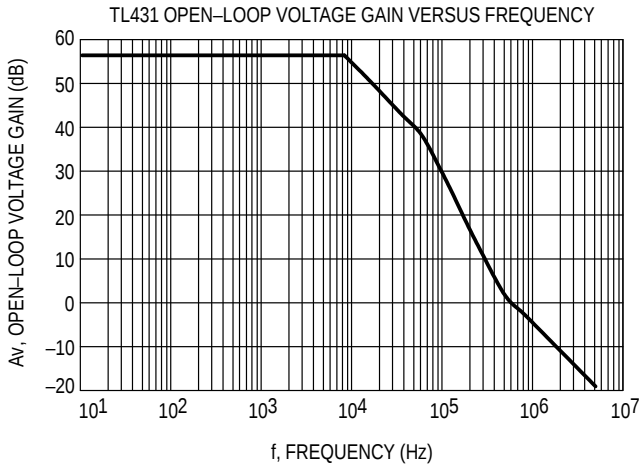


Figure 32. Example 1
Circuit Open Loop Gain Plot



Example 2.

$I_C = 7.5 \text{ mA}$, $R_L = 2.2 \text{ k}\Omega$, $C_L = 0.01 \text{ }\mu\text{F}$. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_O R_L = (2.323)(1.0 \text{ M})(1.25 \text{ }\mu)(2200) = 6389 = 76 \text{ dB}$$

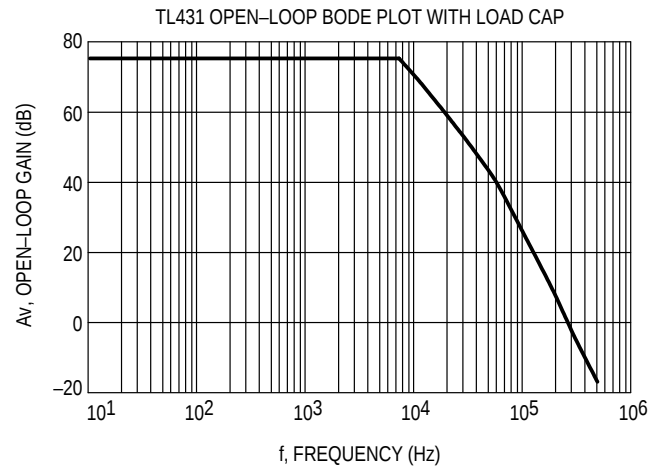
The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(\frac{1 + jf}{500 \text{ kHz}} \right)}{\left(\frac{1 + jf}{8.0 \text{ kHz}} \right) \left(\frac{1 + jf}{60 \text{ kHz}} \right) \left(\frac{1 + jf}{7.2 \text{ kHz}} \right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about -46 degrees. Therefore, instability of this circuit is likely.

Figure 33. Example 2
Circuit Open Loop Gain Plot

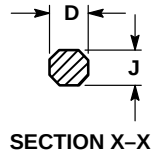
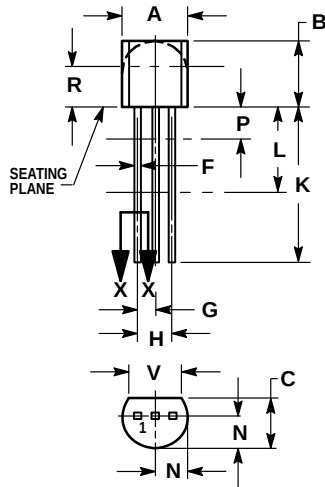


With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

TL431, A, B Series

OUTLINE DIMENSIONS

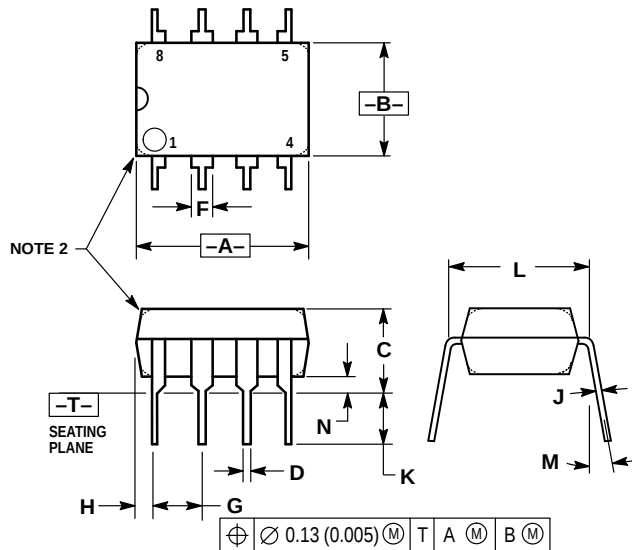
LP SUFFIX PLASTIC PACKAGE CASE 29-04 (TO-92) ISSUE AE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
 4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

P SUFFIX PLASTIC PACKAGE CASE 626-05 ISSUE K



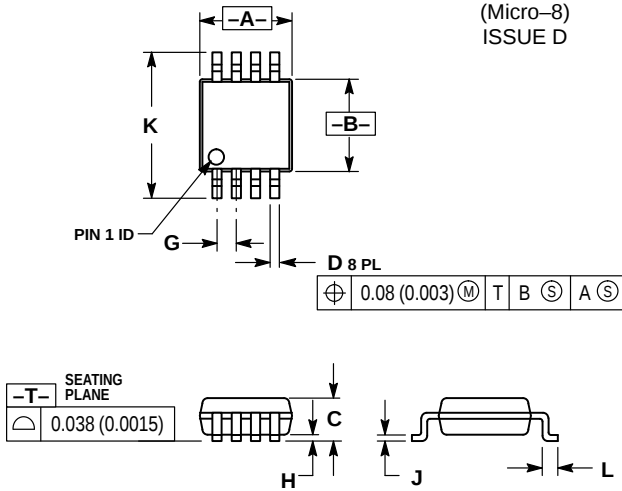
- NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC	—	0.100 BSC	—
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC	—	0.300 BSC	—
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

TL431, A, B Series

OUTLINE DIMENSIONS

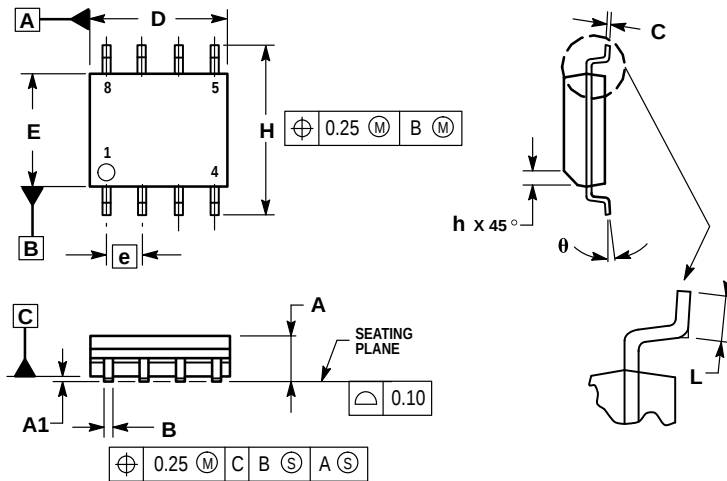
DM SUFFIX PLASTIC PACKAGE CASE 846A-02 (Micro-8) ISSUE D



- NOTES:
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 7. CONTROLLING DIMENSION: MILLIMETER.
 8. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 9. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

D SUFFIX PLASTIC PACKAGE CASE 751-06 (SOP-8) ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS ARE IN MILLIMETER.
 3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
theta	0°	7°